PVP 14

Code: EC3T6, EE3T6

II B.Tech - I Semester – Regular/Supplementary Examinations
November - 2018

SWITCHING THEORY AND LOGIC DESIGN

(Common for EEE, ECE)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Convert $(2468)_{10}$ to $(\ )_{16}$.
b) State and prove consensus theorem.
c) What are the advantages of tabulation method over K-map.
d) Convert the given expression into canonical SOP form
   F = AB+BC+CA
e) Why do go for priority encoder rather than normal encoder?
f) Implement the following functions using Demultiplexer.
   $F1(A,B,C)=\sum m(0,3,7)$ $F2(A,B,C)=\sum m(1,2,5)$
g) Write a brief note on PLDs.
h) Give the comparison between Combinational and Sequential circuits.
i) Convert D-flip flop into SR flip flop.
j) Draw and explain Moore model.
k) Write the limitations of the state machines.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Explain the concept of positive logic and negative logic. Also draw the truth tables for positive logic AND gate and negative logic OR gate. 8 M

b) Obtain the dual of the following Boolean expressions

i) $AB + \overline{AC} + A\bar{B}C$

ii) $\overline{A}\,\overline{B}\overline{C} + \overline{A}\,B\overline{C} + A\,\overline{B}\overline{C} + AB\overline{C}$ 8 M

3. a) Draw the multiple level NOR circuit for the following expression: 8 M

A(B + C + D) + BCD

b) Draw a NAND logic diagram that implements the complement of the following function. 8 M

F(A,B,C,D) = ∑(0, 1 ,2, 3, 4, 8, 9, 12)

4. a) Implement the following Boolean functions using PROM

F_1 (A, B, C) = ∑m (0, 1, 2, 4)

F_2 (A, B, C) = ∑m (0, 5, 6, 7) 8 M

b) Discuss a few applications of multiplexers and distinguish between multiplexer and decoder. 8 M

5. a) Explain the operation of negative edge triggered J-K -flip-flop with active low preset and clear using NAND gates. Give its truth table. 8 M

b) What is shift Register? Draw the block diagram and timing diagram of a shift register that shows the serial transfer of information from register A to register B. 8 M

6. a) Design a serial adder based on Mealy model. 8 M

b) Write down the steps involved in Synchronous sequential machines. Explain it with example. 8 M